ABSTRACT

The invention relates to a DC/DC converter including an input to which an input voltage Vin is applied, a inductance L whose one terminal is connected to the input, a first controllable switch N1 via which the other terminal of the inductance is connectable to a reference potential Vss, a second controllable switch P1 via which the other terminal of the inductance is connectable to the output of the converter, and a regulator circuit 1 configured so that it is able to control the two switches in regulating the output voltage of the DC/DC converter to a predetermined wanted value. The second controllable switch is a PMOS-FET. The regulator circuit is configured so that when the input voltage is higher than the desired value of the output voltage, the gate of the PMOS-FET is permanently connected to a voltage which is larger than the difference between the input voltage and the threshold voltage of the PMOS-FET, it connecting the back gate of the PMOS-FET permanently to a voltage which is larger than the expression input voltage plus threshold voltage of the PMOS-FET minus the diode voltage of a pn junction of the PMOS-FET and timing the first controllable switch with a specific duty cycle so that the output voltage attains the wanted value. The converter in accordance with the invention now permits achieving both an increase and decrease in the input voltage. It can be put to use preferably in conjunction with battery-powered devices for which a wanted voltage is specified.